

ABSTRACT OF THE DISCLOSURE

Sub
A1

includes a stage latch circuit and a stage latch circuit provided at an input stage of a first processing stage for holding a first processing data SOURCE₁ and a second processing data respectively; an operator provided at the first processing stage, for executing a processing by using the first processing data SOURCE₁ and the second processing data; a stage latch circuit provided between the first processing stage and a second processing stage, for holding an output value of the operator; an operator provided at the second processing stage, for executing the processing by using a value of the stage latch circuit when an instruction has been decoded; and an instruction decoder that decodes the instruction to the operator as a through instruction to pass the value of the stage latch circuit through this operator.

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